MEMORY SYSTEM HAVING STUB BUS CONFIGURATION

ABSTRACT OF THE DISCLOSURE

A memory system having a stub-bus configuration transmits a free-running clock through the same path as data signals. A single clock domain is employed for both read and write operations. For both operations, the read or write clock signal is routed through the same transmission path as the data, thereby increasing system transfer rates by maximizing the window of data validity. In this manner, data bus utilization is increased due to the elimination of a need for a preamble interval for the strobe signal, and pin count on the memory module connectors is therefore reduced.

J:\SAM\0204\204PATAPP3_WORD.DOC